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09/989,931	11/21/2001	Fernando Gonzalez	MI22-1801	1568

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EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 01/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/989,931	GONZALEZ ET AL.	
	Examiner	Art Unit	
	José R Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14-30 and 57-60* is/are pending in the application.

4a) Of the above claim(s) *2,4 and 5* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,6-12,14-30 and 57-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: the proposed reference sign "51". A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "52" has been used to designate both "isolation region" (fig. 7) and "exposed portion 52 of mass 16" (fig. 8). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 1, 3, 6-12, 14-30 and 57-58 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1; 16, 57 and 58 recite the limitation "the providing step" after the limitation of "at least partially filling the recess with a semiconductor material...other than silicon." There is insufficient antecedent basis for this limitation in the claim.

Claims 3, 6-12, 14-15, and 17-30 are rejected due to their dependency on claim 1 and 16, respectively.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 3, 14-19 and 59 are rejected under 35 U.S.C. 102(e) as being anticipated by Furukawa et al. (US Pat. No. 6,555,891 B1).

Regarding claim 1, Furukawa et al. teaches a method of forming semiconductor circuitry, comprising: providing a monocrystalline silicon substrate (12, 15) (see fig. 3); forming a mask (17) which covers a first portion of the substrate (consider the regions adjacent to the trench 20) and leaves a second portion uncovered (consider the region wherein the trench 20 is formed) (see fig. 3); forming a recess (20) in the uncovered portion (see fig. 3); after forming the recess (20), providing an insulative material spacer (22) along a sidewall of the recess (see fig. 4); at least partially filling the recess (24)

with a semiconductive material that comprises at least 1 atomic percent of an element other than silicon (SiGe) (see fig. 5 and col. 4, lines 57-60), the providing step being performed before at least partially filling the recess with the semiconductive material, wherein the at least partially filling the recess with the semiconductive material comprises providing the semiconductive material along the insulative material spacer (see fig. 5); removing the mask (17) (see fig. 6); forming a first semiconductor circuit component (90A, 90B) over the first portion of the substrate (see fig. 11); and forming a second semiconductor circuit component (55) over the semiconductive material that at least partially fills the recess (see fig. 11).

Regarding claim 3, Furukawa et al. teaches that the substrate comprises a monocrystalline silicon mass (15) over an insulative material (16), and wherein the recess is formed within the monocrystalline silicon mass (see fig. 3).

Regarding claim 14, Furukawa et al. teaches that the insulative material comprises silicon nitride (22) (see col. 4, lines 13-14).

Regarding claim 15, Furukawa et al. teaches that the insulative material (22) comprises silicon dioxide (see col. 4, lines 11-13).

Regarding claim 16, Furukawa et al. teaches a method of forming semiconductor circuitry, comprising: providing a substrate comprising a first monocrystalline material (12), an insulative layer (16) over the first monocrystalline material, and a second monocrystalline material (15) over the insulative layer and spaced from the first monocrystalline material by at least the insulative layer (see fig. 1); the second monocrystalline material (15) consisting essentially of a first element (Si) (see col. 4,

lines 57-60); forming a mask (17) to cover a first portion of the second monocrystalline material (consider the regions adjacent to the trench 20), while leaving a second portion uncovered (consider the region wherein the trench 20 is formed) (see fig. 3); removing at least some of the uncovered portion to form a recess (20) (see fig. 3), after forming the recess (20), providing an insulative material spacer (22) along a sidewall (22) of the recess (see fig. 4); at least partially filling the recess with a semiconductive material (24) (see fig. 5) that comprises at least 1 atomic percent of an element other than the first element (Ge) (see col. 4, lines 57-60), the providing step being performed before at least partially filling the recess with the semiconductive material (see fig. 5) wherein the at least partially filing the recess with the semiconductive material comprises providing the semiconductive material along the insulative material spacer (see fig. 5); removing the mask (17) (see fig. 6); forming a first semiconductor circuit component (90A, 90B) over the first portion of the second monocrystalline material (see fig. 11); and forming a second semiconductor circuit component (55) over the semiconductive material that at least partially fills the recess (see fig. 11).

Regarding claim 17, Furukawa et al. teaches that the first and second monocrystalline materials (12, 15) consist essentially of silicon (see col. 3, lines 1-6).

Regarding claim 18, Furukawa et al. teaches that the first and second monocrystalline materials (12, 15) consist essentially of silicon (see col. 3, lines 1-6), and wherein the insulative layer (14) consists essentially of silicon dioxide (see col. 3, lines 5-8).

Regarding claim 19, Furukawa et al. teaches that the mask (17) comprises a layer consisting essentially of silicon nitride (18) over a layer consisting essentially of silicon dioxide (19) (see fig. 2).

Regarding claim 59, Furukawa et al. teaches a method of forming semiconductor circuitry, comprising: providing a monocrystalline silicon substrate (12, 15) (see fig. 1); forming a mask (17) which covers a first portion of the substrate (consider the regions adjacent to the trench 20) and leaves a second portion uncovered (consider the region that include the trench 20) (see fig. 3); forming a recess (20) in the uncovered portion (see fig. 3); at least partially filling the recess with a semiconductive material (24) that comprises at least 1 atomic percent of an element other than silicon (Ge) (see col. 4, lines 57-60); removing the mask (17) (see fig. 8); forming a first semiconductor device component over the first portion of the substrate (90A, 90B) (see fig. 11); and forming a second semiconductor circuit component, that is different from the first semiconductor device component, over the semiconductive material that at least partially fills the recess, wherein the first semiconductor device is incorporated into a DRAM array, and the second semiconductor device is incorporated into logic circuitry corresponding to a portion of circuitry formed peripheral to the DRAM array (see col. 7, lines 18-24).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 6-10, 20-26, 57-58 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa et al. (US Pat. No. 6,555,891 B1) in view of Liaw et al. (US Pat. No. 5,891,769).

Regarding claims 6-10, 20-26, 57-58 and 60, Furukawa et al. fails to teach that the semiconductor material comprises essentially of III/V compound semiconductive material; silicon and at least 1% carbon, or silicon and 1%-20% Ge.

However, Liaw et al. teaches that III/V compound semiconductive material (i.e. GaAs and GaN), silicon and at least 1% carbon (e.g. SiC), silicon and 1%-20% Ge (e.g. SiGe) are well known semiconductive materials used in the art to enhance the carrier mobility within the channel (see col. 1, lines 20-21, col. 3, lines 32-33, and col. 5, lines 40-43

Furukawa et al. and Liaw et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would

have been obvious to a person of ordinary skill in the art to form a semiconductor material comprising III/V compound semiconductive material, silicon and at least 1% carbon, or silicon and 1%-20% Ge. The motivation for doing so, as is taught by Liaw et al., is for improving carrier mobility within the channel (col. 1, lines 20-21). Therefore, it would have been obvious to combine Liaw et al. with Furukawa et al. to obtain the invention of claims 6-12, 20-26, 57-58 and 60.

10. Claims 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa et al. (US Pat. No. 6,555,891 B1) in view of Liaw et al. (US Pat. No. 5,891,769), and further in view of Wang et al. (US Pat. No. 6,620,671 B1).

Regarding claims 27-28, Furukawa et al. teaches that the semiconductor is SiGe that is planarized by a CMP process (see 4, lines 57-60 and col. 5, lines 4-5).

However, a further difference between the prior arts and the claimed invention is the further step of performing a rapid laser annealing at a temperature of about 800 °C – 1100 °C. Wang et al. teaches it is well known in the art to anneal the SiGe semiconductor material by a rapid thermal annealing process at a temperature of about 800 °C –1100 °C (see 5, lines 15-39).

Furukawa et al., Liaw et al. and Wang et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to rapid laser anneal the SiGe semiconductor material at a temperature of about 800 °C –1100 °C. The motivation for doing so, as is taught by Wang et al., is crystallize the semiconductor

material (col. 5, lines 15-17). Therefore, it would have been obvious to combine Wang et al. with Furukawa et al. and Liaw et al. to obtain the invention of claims 27-28.

Response to Arguments

11. Applicant's arguments with respect to claims 1, 3, 6-12, 14-28 and 57-60 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

12. Claims 29 and 30 would be allowable if rewritten to overcome the rejection under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to teach, disclose, or suggest, either alone or in combination, a method of forming a semiconductor circuitry having a semiconductor material that partially filled a recess, wherein the semiconductor material includes silicon (Si) and an atomic concentration of from about 1%-20% of germanium (Ge), the SiGe semiconductor material is polished by a CMP process to form a planarized surface which extends across the semiconductive material and mask, and after the CMP process, the SiGe semiconductor material is further laser annealed; and wherein the mask is removed after the laser annealing step.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wallace et al. (US 20030062586 A1) discloses growing an epitaxial SiGe layer (see fig. 1b) and then, forming a device on said SiGe layer (see fig. 1e); Puchner (US 006544854 B1) discloses SiC CMOS channel and laser annealing (see abstract); Stecki et al. (US 005759908 A) discloses method for forming SiC and GaN on a SOI substrate (see fig. 1); Chu et al. (US 20020182423 A1) discloses a method of growing SiC and SiGe (see abstract); and Matsumura et al. (US 20020086557A1) discloses a method for forming SiGe, SiC and III-V compound material (see paragraph [0053].

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (703) 308-6078 or (571) 272-1727, after February 9, 2004. The examiner can normally be reached on 9:00-5:00 Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Tom Thomas

JRD